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Communication Protocols Augmentation in VLSI Design Applications

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Abstract—
With the advancement in communication System, the use of various protocols got a sharp rise in the different applications. Especially in the VLSI design for FPGAs, ASICS, CPLDs, the application areas got expanded to FPGA based technologies. Today, it has moved from commercial application to the defence sectors like missiles & aerospace controls. In this paper the use of FPGAs and its interface with various application circuits in the communication field for data (textual & visual) & control transfer is discussed. To be specific, the paper discusses the use of FPGA in various communication protocols like SPI, I2C, and TMDS in synchronous mode in Digital System Design using VHDL/Verilog.

Index Terms—Digital, FPGA, Interface, I2C, Protocols, Software Augmentation, SPI, TMDS, VHDL,

1.0 INTRODUCTION

The FPGAs (Field Programmable Gate Arrays) has played an important role in the system design. This provides a path for a simple design to be mapped into the FPGA building blocks which further decomposed into various functional circuits. The use of VHDL helps in programming various processes & functions which gets optimized. Then, the synthesis makes the design check easier through simulation software's. To do so, input output modules are written for the design. There are various methods like built in self test(BIST) are implemented to test design using the scan design & boundary scan design methodology. It has been discussed in a nut shell the use of SRAM, EEPROM & using SPI/I2C models using VHDL. THE TMDS encoding techniques is also brought out for VDI data transfer.

2.0 DESIGN ELEMENTS

2.1FPGAs:

The complexity of the digital system design the discrete Integrated circuits find it difficult, which then found to be realized through ASICS (Application Specific Integrated Circuits) , and FPGA (Field Programming Arrays) . The design got simplified by the use of Hardware Language tools like VHDL & Verilog and other high level languages like System C. As the name suggests that VHDL is a Very High Speed Integrated Circuits,(VHSIC) Hardware Description Language, got approved by ANSI (American National Standard Institute) and regarded as VHDL. It has become a very popular tool both for Industry & academic sectors. There are various versions of this language and latest version is named as ieee.std_logic_1164 version. This paper is written for the design of VLSI circuit & implementation through the use of VHDL algorithms on FPGA CSG324 on Xilinx platform, Saturn Spartan6 FPGA on board. This is done through a hardware tool of Xilinx USBII cable, JTAG interface. The other devices have been selected are memories like FRAM,SRAM, TMDS Modules and other associated hardware & software.

2.2 Language (VHDL)

The language, VHDL has been divided into two constructs such as Entity (ii) architecture. The entity is a pre defined word and the architecture is a relationship between input & outputs of the systems bound to the entity. This binding helps in the visibility of the entity to the architecture. The system can be designed with the use of VHDL language on the Xilinx platform, FPGA being as the target device where the application program can be stored for the purpose of application devices.

2.3 Communication Protocol

In this kinetic world, the present requirement needs the systems to be controlled by a programmed manner in order to keep pace with the shortest time interval. Such transfers of our data & control signals are only possible by various communication modes so far developed. To enact such dynamic movements of data/controls to the application devices by a controller/master device, the path for the communication need to be selected suitably. Hence, there are some protocols in our communication systems that have been devised. to transfer/control the transition minimization of data and the control signal

transfer. Such communication protocols like SPI (Serial Peripheral Interface) / or I2C (Inter Integrated Circuit) &TMDS (Transition Minimized Differentiation Signaling) protocols. It has been found to very useful even in our Missile/aircraft application like Tomahawk Missile systems. The following sections are described with the interface of FPGAs with the application circuits with use of the protocols.

2.3.1 SPI Protocol

The SPI Protocol is Serial Peripheral Interface works in the synchronous mode of communication. It uses the 4 wires/3-wires bus between the master & slave devices to transfer the data and control signals through individual lines. Hence it becomes simpler in the design of interface. Those bus lines are named as MOSI (Master Out &Slave In) ,MISO(Master IN Slave Out), SCLK(Serial Clock) and the SS(Slave Select). The master (Device) can be interfaced with many slaves (devices) controlled though Slave Select line. This protocol can be used in 4 modes. However, preferably, this is used with the use of 2 modes i.e., Mode 00 (0) & mode 11(3) .Mode 00 means the data transfer takes place during the SCLK in Phase 0, Polarity 0 in mode(00b) 0d, & SCLK in Phase 1 & polarity 1(11b) 3d in mode (11b) ,3d.

(i) Presently it is used in the missile/avionics sectors (e.g., ref: Tomahawk missile).

(ii) SPI protocol is being used for the control application of Gyroscopic sensor modules.(ref: CSE 260M Lab5)

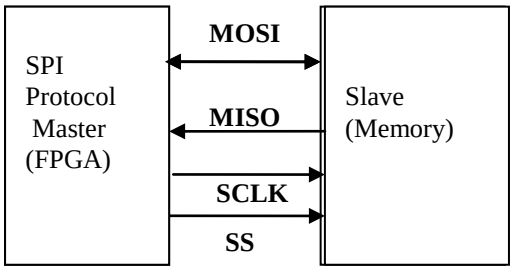

Fig:2 SPI Protocol

2.3.2 I2C(Inter Integrated Circuit) Protocol

The I2C communication protocol is another important one in the synchro mode. It uses only two wires bus, i.e.,(i) SDA(Serial Data) & (ii) SCL (Serial Clock). The SDA line is bi-direction one where as the SCL clock generation line. This interface facilitates many masters & many slaves controlled through an acknowledge mode of acceptance/hold/ with start & stop bit signal conditions.IN case of multiple master situations, the master having their own clock generation systems, the devices are connected in the Wired-AND conditions , thereby the data collision of two or more masters are avoided. This is done through various techniques like Arbitration techniques & Handshake conditions of synchronization. This mode is complex as compared to SPI mode. However due to its other advantages like low & medium speed requirements these are used for on-board chips/application circuits.

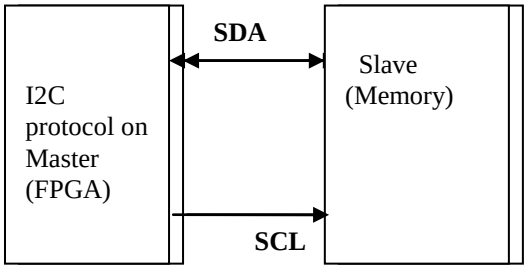

Fig: 2.2 I2C Protocol

2.3.3 TMDS (Transition Minimization Differential Signaling) :

This is another method called TMDS technique of data conversion & transfer of visual data & control signals between the master & slave devices for the application purposes. It is also called the TMDS coding standard. The communication is done through the various processes like phase detection, coding schemes using 8Bit to 10Bits with the word and speed synchronization techniques. As the name signifies the differential signaling method which is achieved through the transmission of 1s & 0s in the same single lines with it's opposite values, thereby reducing the EM Interference.

The visual data is transferred from the transmitter with the help of TMDS encoder & the same data is received by a decoder by decoding techniques at the receiver. The processes uses, which are called as serializer & deserializer methods by the 8B/10B coding technique

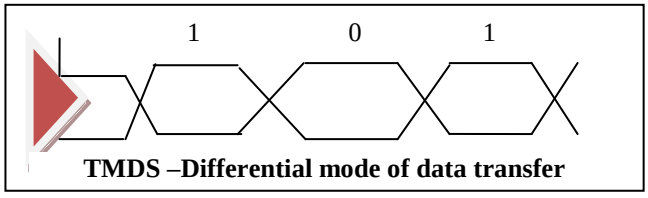

Fig: 2.3 TMDS Protocol

The receiver subtracts one signal from the other and thus cancelling any noise and recovers the data. TMDS encoding uses three RGB data channels & one clock channels. The data is. Thus the parallel data is serialized & at the transmitter end & de-serialized at the receiver end. This DVI (Digital Visual Interface)

is preferred over VGA, due to its noise immunity , which is achieved through differential signaling techniques & zero dc component by dc balancing techniques during digital video transmission. This protocol has been developed by DDWG (Digital Display Working Group). In this system, there are two possible links. One is Primary (i.e., Link#0) and other is secondary (Link#1). However, during transmission, the TMDS Link #0 is also available for service, and Link#1 is active only when there is demand for pixel forms & timing requirement becomes greater than 165 Mhz. This TMDS interfaces between the FPGA and any LCD Device.

3.0 Digital System Design

The design elements as discussed is put into use in a suitable manner as to provide the necessary input & and Output conditions after being processed. The systematic process of helps to constructs circuits design by meeting the requirements & the specifications. In particular VLSI (Very Large Scale Integration) of electronic circuits has been found to very useful in the field of communication. Any project to start with has to be defined by top level description of the specifications. The system specification then becomes useful in determining abstract, the high-level model. The abstract modeling has to be done by a hardware language and it done either by VHDL or Verilog. The abstract model reflects the behavior information of each block & their functions. A digital system can be described by it's abstraction right from the architecture level to the gate level. The simulations semantics are associated with all such HDL packages to enable verify the correctness of the design. The synthesis process of the model enables the translation exercise bringing out a net list, which maps in the form of RTL blocks /gate levels circuitry.

4.0 Built In Self Test (BIST)

The design will be incomplete without a Built in Self Test (Check) embedded into it. It is more generally used for memory by logic in built into the device. The process involves a test pattern which is compared with a Device under Test (DUT). The general architecture of the BIST for a RAM is depicted below for ref.

The circuit shown with the controller enables the write generator & address counter to write data to the specific location of the DUT. After which the Address generator & Read generator are enabled the data to be read from each of the device locations. It is then compared with the Read generator check board patterns (alternating 0's & 1's) for its correctness. The error is then fed back through the feedback circuits to the controller for correction. The process , let us say write alternate 0's & 1's in all even addresses and alternating 1's & 0's in all odd addresses. Then the odd & even addresses are swapped to complete the test. The process is repeated until the correct data is read. There are different ways of testing the DUT.

To name them, March test for a RAM in which each cell is read and its complemented value is written. The process is continued until it covers the entire memory. Similarly, the test is repeated in the reverse order. In another method, the test circuit uses a signature in which the output data is compressed to a short string of bits, which is then compared with that of another signature of a correct device. This test can be used with a multiple input signature register (MISR) in which the read generator & comparator can be eliminated. In another form of MISR uses the check-sum method.

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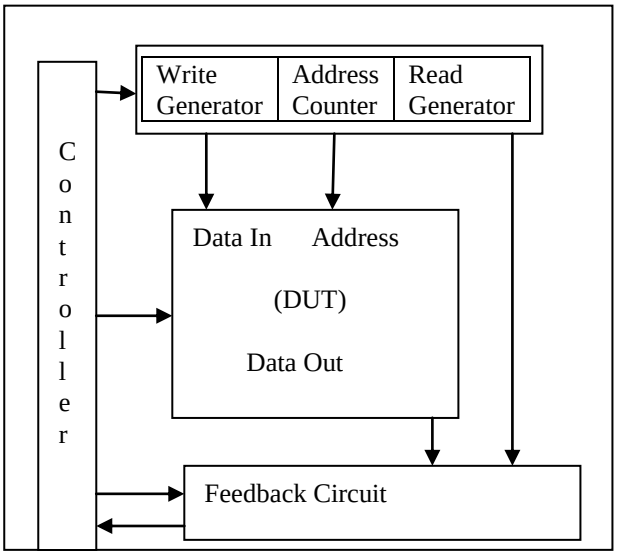

Fig.4.1 BIST (Built In Self Test) Architecture

There is another method called Linear feedback shift registers (LFSRs), in which a test pattern is generated and out is compressed into signatures. This uses a shift register with two or more F/F outputs XOR'ed (modulo-2) together and fed back to the first Flip Flop. The bit positions that are affected are called taps. So, in this 2^n -1 different bit patterns can be generator using n-bit shift register. (e.g., 1100. 1110.. etc.). However, the all 0's patterns cannot be generator

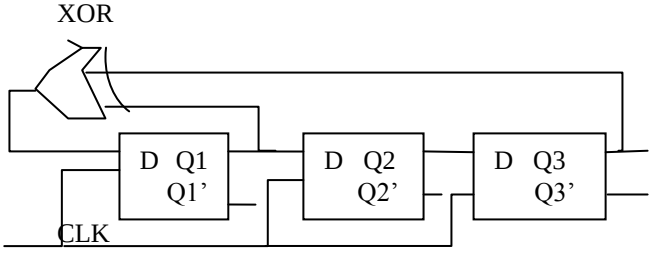

Fig.4.2 LFSR (Linear Feedback Shift Registers)

There are few more self test methods like pseudo-random pattern generator (PRPG) in the BIST circuit, STUMPS (Self Test using MISR & Parallel SRSG (Shift Register Sequence Generator), BIST using BILBO (Built In Logic Block Observer) technique etc. Accordingly, the VHDL codes can be generated for each type test.

5.0 Software -Design

The digital system design is nothing but the embedded systems, which forms a part or many parts in a simple or complex system. The program can be a high level like C or C++ or any hardware language (HDL) like VHDL/or Verilog. However, the complexity of high level language restrains the use by many of designers; rather they prefer to use HDL languages. Hence, it is felt that the use of VHDL helps in the verification process in various stages to ensure the correctness of the stages before entering to the next.

6 .0 Design Model

A model of a digital circuit is an abstract by a modeling language. Such a language is preferred here to VHDL/ Verilog. However, the object oriented language like C++ has an extension to it, called System C, to be one such language, which could be used for this purpose too.

7.0 Software Augmentation

Although many authors has spelt out various design methods, however, the recent methodology is the process of augmentation of the application software into the hardware (application circuit/device) itself. The application software developed for any application devices is programmed & stored in a memory (slave Device) though the FPGA (target device) on any Software Plat form like Xilinx. The FPGA has been embedded into a Spartan6 Xilinx Platform. The memory could be any on board SRAM, or any external SRAM, and the display device could be a LCD/or SSD/or LEDs. This could be done as described below: The very initial step is to perform the study of requirements and done the analysis for both hardware and software essentialities & constraints. Then the hardware & software constraints are resolved. Once the constrains are removed, the hardware design is performed, As a concurrent mode, the software is to be made ready. The paper discussed here has been chosen for the FPGA on Spartan6 Xilinx platform. The HDL has been selected as VHDL. The application software has been prepared accordingly. Last but not the least, is the augmentation of software into the application devices. Our co authors have already selected various sensors for their applications. Accordingly, the program has been verified through the built in ISim software tools for the proper timing and correctness of the design. This paper is is a reflection of the collective effort of our engineers for their projects, on Modeling & Implementation of various communication Interfaces using VHDL at KCTRONICS Innovative Services Private Limited, Bangalore..

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